

GOVERNMENT OF TELANGANA

**OFFICE OF THE
COMMISSIONER OF TECHNICAL EDUCATION
TELANGANA::HYDERABAD**

Cir. Memo No. T/ General /2015

Date: 01.12.2017

Sub: Technical Education – Recruitment of Junior engineer trainees
from Polytechnic – Reg.

Ref: The mail received from Prof. K. Subbarangaiah, SoCtronics
(VEDAIIT), Hyderabad

With reference sub cited, the Principals of Government Polytechnics in the state are informed that VEDAIIT, Hyderabad, proposes to conduct Pool Campus Drives for the following positions in the consortium companies in VLSI core domain of Junior engineer trainees for Diploma holders in ECE / EEE / IE / Computer Science / Instrumentation. The following is the schedule.

Test	Eligibility	Date & Time
Prelim	Approved candidates with hall ticket	16/12/2017 :09 AM to 10 AM+
Main	Short-listed candidates in prelim	16/12/2017 : 04 PM to 06 PM
Interview	Short-listed candidates in Main	17/12/2017 : 09 AM to 07 PM#

In this connection, All the Principals of Government Polytechnic are hereby informed to ensure maximum participation and also bring to the notice of students about six(6) months of apprenticeship / Training, Company sponsored knowledge-intensive, industry-oriented full-time training at VEDA IIT (Stipend will be paid during apprenticeship). Interested students may apply at www.vedaiit.org. Registration fee for pass-outs is Rs. 300/-. Last date for application is 11th Dec 2017. No fees for campus students who apply on-line with 'valid coupon code' by 11th Dec 2017.

Encls: As above

Sd/- A. VANI PRASAD
COMMISSIONER

To
All the Principals of Government Polytechnics., TS.
Copy to the Secretary, SBTE&T., Hyderabad
Copy to the RJD (TE), Hyderabad.
Stock file/ spare copy.

//F.B.O.//

A. Vani Prasad
SUPERINTENDENT
04/12/17

Junior Engineer Trainees Recruitment

Challenging work opportunities for
Polytechnic/B. Sc. Candidates
at

SoCtronics

in core domains

VLSI Design & Engineering

- Logic Design
RTL Design, Implementation, Verification & DFT
- Physical Design
Physical Placement & Routing,
Functional Equivalence, Timing Closure
and Design Rule Check
- Standard Cell Design
FOM Analysis, Architecture, Design Optimization,
Characterization, PPA, Bench Marking
- Custom Layout Design
Custom layout design of high performance
Analog Circuits, Layout verification

Embedded System Design & Engineering

- Embedded Software Development
Firmware/ Drivers/ Multimedia SW for Mobile,
Wearable and IOT Systems
- Software Testing
Automation, Testing & QA for Embedded SW,
Systems & Applications
- System Engineering
Platform Engineering, HW/Board Design, Silicon
Validation/ Characterization
- Application Software Development
Software Development for Web, Embedded System
and Engineering Applications

ELIGIBILITY : i) Diploma in Electronics/ Electrical/ Communications/ IE/ Computer Science/ Instrumentation
ii) B. Sc. in Electronics
iii) Final year students can also apply

6 months of apprenticeship/training
Company sponsored knowledge-intensive, industry-oriented
full-time training at VEDA IIT
(Stipend will be paid during apprenticeship)

Apply at www.vedaiit.org

Registration fee for Pass-outs: Rs. 300/- Last date for application : 11th Dec 2017*

No fees for campus students who apply on-line with 'valid coupon code'** by 11th Dec 2017

* Application submission can be closed earlier than this whenever the number of applicants exceeds the actual seating capacity at the exam center
** VEDA IIT provides 'valid coupon codes' to TPO/HODs of different colleges on request; Number will be limited to the seating capacity

Test	Eligibility	Date & Time
Prelim.	Approved candidates with hall tickets	16/12/17, 9 AM to 10 AM [†]
Main	Short-listed candidates in Prelim	16/12/17, 4 PM to 6 PM
Interview	Short-listed candidates in Main	17/12/17, 9 AM to 7 PM [#]

† Pre-Placement talk - 16/12/2017, 10:15 AM to 10:45 AM

Interview schedule beyond this date will be intimated on that day



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